| 9 | Library Copy | CSE-JUI |
|-------|---|------------------------|
| 9 | Roll No. : | otal Printed Pages : 3 |
| 8E401 | B. Tech. (Sem. VIII) (Main/Back) Examination Computer 8CS3 Advanced Computer Architecture | on, April/May-2011 |
| | | |

Time: 3 Hours]

[Total Marks: 80

[Min. Passing Marks: 24

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

| 1. <u>Nil</u> 2. <u>Nil</u> | 2. <u>Nil</u> | 1. NII | | 1 |
|-----------------------------|---------------|--------|--|---|
|-----------------------------|---------------|--------|--|---|

- 1 (a) Explain with an example the parallel processing mechanisms in uniprocessed systems.
 - (b) Explain Flynn's classification of Computer Architecture.

OR

- 1 (a) Write short notes on:
 - (i) PRAM Models
 - (ii) VLSI Complexity Model ~

(b) A 40 M-Hzs. processor was used to execute a benchmark program with the following instruction mix and clock counts;

| Instruction type | Instruction Count | Cock Cycle Count | | |
|--------------------|-------------------|------------------|--|--|
| Integer Arithmetic | 45000 | 1 | | |
| Data Transfer | 32000 | 2 . | | |
| Floating Point | 15000 | 2 | | |
| Control Transfer | 8000 | 2 | | |

Determine the effective CPi and MiPS rate for this program.

8

2 (a) What is memory interleaving? Explain C-access and S-access memory organisations.

(b) How does a linear pipeline processor work? Define and desire the formula for speedup, efficiency and throughput.

2 Consider the four state static multifunctional pipelined processor specified by the following reservation table:

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|-------|-------|
| S_1 | Α | | В | 1 | | В |
| S_2 | | В | A | | N. E. | A |
| $egin{array}{l} \mathbf{S}_1 \\ \mathbf{S}_2 \\ \mathbf{S}_3 \\ \mathbf{S}_4 \end{array}$ | | A | 8 | В | A | ate . |
| S_4 | В | | | A | В | |

- List the set of forbidden latencies and the initial collision **(i)** vector.
- Draw a state transition diagram for scheduling the pipeline. (ii)
- (iii) List all simple cycles from the state diagram.
- (iv) Identify the greedy cycles among the simple cycles.
- Determine the optimal constant latency cycle and the minimal (v) average latency.
- 3 Describe at least four characteristics of MiMD multiprocessors (a) that distinguish them from multiple computer systems or computer networks.

What are various levels of parallelism in program execution? **(b)** Differentiate between fine, medium and coarse grain.

8

OR

- 3 Describe the following terms related to processor technology: (a)
 - SiMD Interconnection Networks. (i)
 - (ii)Page Replacement policies.

What are various levels of parallelism in program execution.

2

8E4016]

[Contd...

| 4 | (a) | Write short notes on: |
|---|-----|---|
| | | (i) Row Column Oriented Algorithms |
| | | (ii) Block Oriented Algorithms. |
| | | 8 |
| | (b) | Discuss Jacobi Algorithm alongwith its sequential implementation. |
| | | 8 |
| | () | OR |
| 4 | (a) | Explain the algorithm of matrix multiplication for SiMD array processors. |
| | | 8 |
| | (b) | Define various types of PRAM models of parallel computation. |
| | | Write PRAM algorithm to find prefix sums of an n-element list using $n-1$ processors. |
| | | 8 |
| 5 | (a) | Explain various parallel languages constructs. |
| | | • • • • • • • • • • • • • • • • • • • |
| · | (b) | Write short note on master and synchronization directives. |
| | | 8 |
| | | OR |
| 5 | (a) | List out various conditional compilation directives. |
| | | 8 |
| | (b) | Discuss combined parallel work-sharing constructs. |
| | | 8 |
| | | |